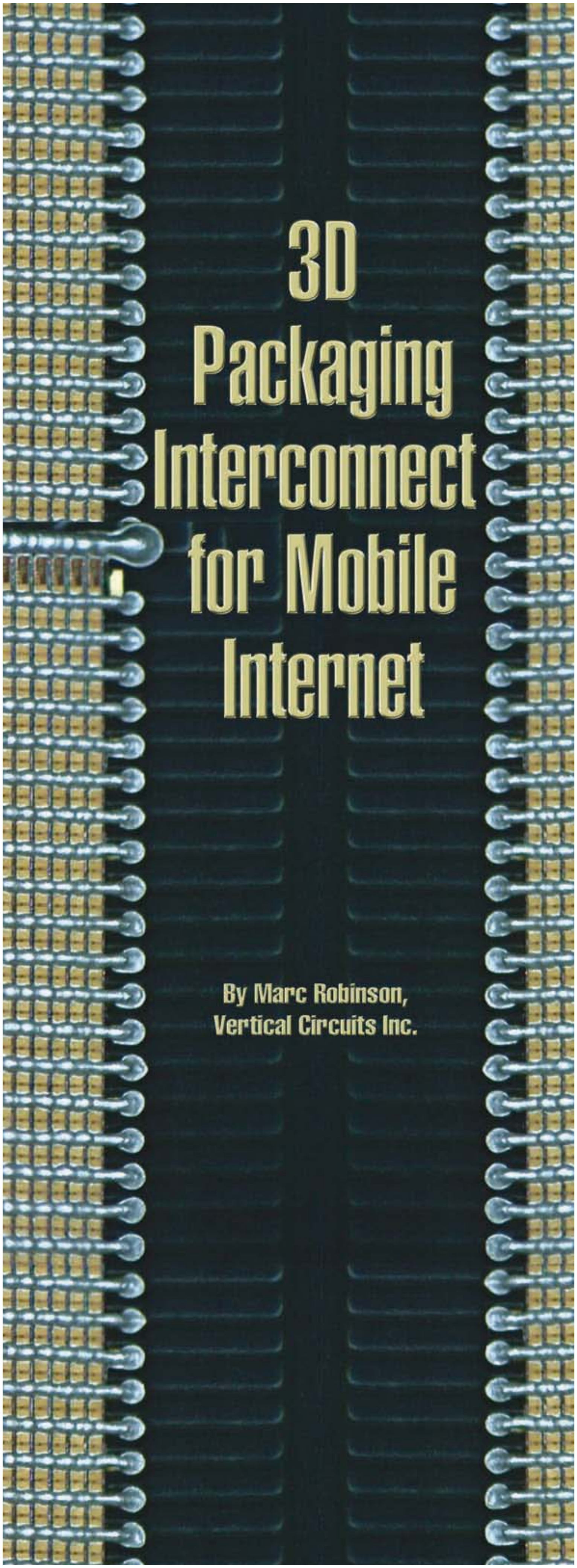

# 3D Packaging Interconnect for Mobile Internet

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3D packaging, TSVs, Solid State Drives, conformal liquids, nanoparticle inks

**A new low cost back-end 3D solution can be a very competitive alternative to TSVs for mobile Internet products**

In 3D applications, interest is exponentially increasing in low cost, easy to implement packaging solutions that integrate increasing amounts of memory and other semiconductor devices in a wide variety of consumer products. A clear convergence of features and functionality is driving requirements for more silicon in smaller form factors. Portability and the desire for instant information access are the key factors in the adoption of new, innovative packaging solutions.

Today's users are unwilling to wait for their PCs and Macs to boot up to access email or the web. Instead, new handheld devices – loaded with enhanced capabilities – now provide instant Internet access, 24/7. Engineers and designers are trying to squeeze smart phones, digital cameras, music players, GPS systems and other electronic devices with significant amounts of memory into a single, small package with unlimited battery life. New product categories, such as netbooks and solid state drives (SSDs), will benefit greatly from 3D packaging solutions, contributing significantly to the mobile Internet experience.

While much interest and activity are directed toward through silicon via (TSV) solutions, many obstacles exist to widespread TSV adoption. As memory devices move from one lithography node to the next, the die get bigger at each successive generation, even though the area per bit shrinks, because of the memory progression to larger capacities per die. This increases end-product costs, as many TSV costs are wafer based, and hence the cost per die will increase as increases in die size reduce the number of die per wafer.

Memory die also have a relatively low number of I/Os per device. So from a cost per I/O perspective, the impact is even greater; 5-10× wire bond equivalent cost (see **Figure 1**). Furthermore, TSV equipment is very expensive and will limit TSV's adoption to the largest manufacturers, which will apply TSV to the largest volume chips. Even then, standardization and availability issues are expected to severely limit TSV adoption.

Will processor and memory suppliers agree on the location of vias on all die so that die from different vendors can be stacked in the same package using TSVs? Where will the responsibility for yield loss lie, and who will take the financial hit? Due to these and other business issues, TSV will likely be adopted within single manufacturers for products built with all die from the same manufacturer.

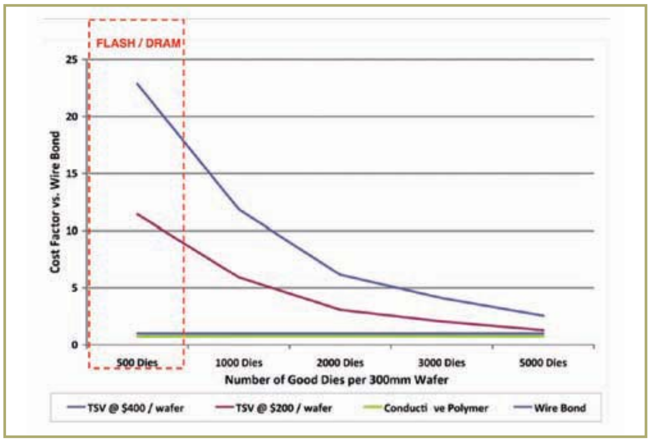


**Figure 1.** TSV and conducting polymer cost vs. wire bonding.

This article describes a new interconnect technology platform for mobile Internet convergence. The technology is being used in a wide variety of 3D packaging solutions for small form factor, low cost, consumer electronic devices. Essentially, the approach uses conductors that are applied as conformal liquids to the edges of dies and packages in a wide range of stacking configurations.

Die can be stacked with coincident edges, offset edges or staggered edges. Insulation is applied to the die edges so the conductors can be placed directly against the die side, yielding footprints barely larger than the die. More importantly, the technology can be implemented in back-end assembly facilities and can accommodate die from different manufacturers. Working closely with back-end suppliers, a defined supply chain has been established to take the risk and guesswork out of adopting this new technology.

## Die Stacking Configurations

Coincident edge, staggered edge and offset edge stacks all allow multiple die to share the same board real estate. Coincident edge offers minimum footprint growth, but a means must be provided to access die pads that lie on the top die surface. Typically, a spacer is used between the die that is smaller than the die's area, leaving the die pads exposed, and allowing the edge conductors to reach the exposed die pads from the edge opening between stacked die. This method works well for die that have pads on one, two, three or four sides, but increases total stack thickness. **Figure 2** depicts coincident edge die stacking with conformal inter-die interconnect.

Staggered edge stacks allow each die to act as spacers for the die above and below, exposing one or two adjacent sides of the underlying die. This works well for flash die, as the connection pads are typically on only one side of the die. Alternate die are rotated 180 degrees, and one connection bus is on each side of the stack. As every other die is edge aligned with the die two levels below, the footprint is increased by the offset necessary to expose the pads on one side. By using a conformal liquid conductor, the offsets can be smaller than those required for wire bonded die interconnects.

This method can also be used if the die are not square, by alternating the rotational orientation of successive die in the stack by 90 degrees, thus exposing pads on the short ends. This allows stacking of die with pads on two sides without using spacers. **Figure 3** depicts a stagger stack structure.

Finally, much flash stacking is done whereby each layer is offset from the next to create a stair-step or terraced structure. This also eliminates the need for a spacer between die, allowing for a thinner stack. But it can significantly increase the stack footprint, especially if wire bonds are used. **Figure 4** depicts a stair-step stack and shows the difference in offset between a wire-bond implementation, and the conformal conductor method described in this article.

By using a conformal conductor instead of wire bonds, the footprint growth for an 8-high flash stack was reduced by more than half. An arrow or zigzag stack arrangement can be used to further reduce the terraced stack footprint by switching the direction of the die offset for the die in the top half of the stack

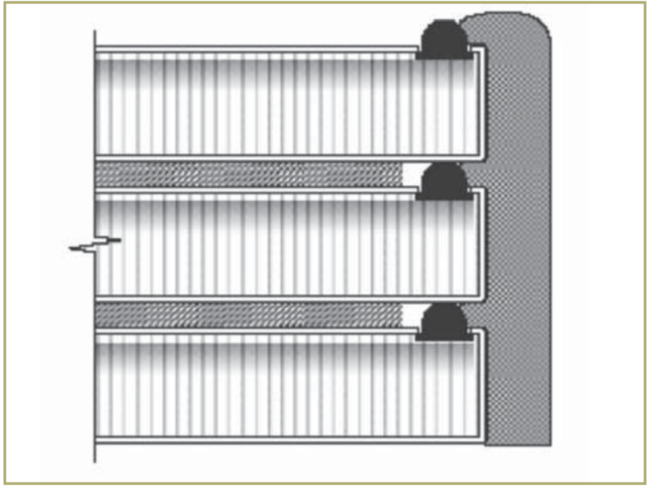


**Figure 2.** Coincident edge die stacking with spacers.

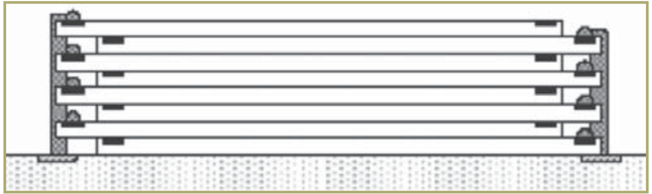
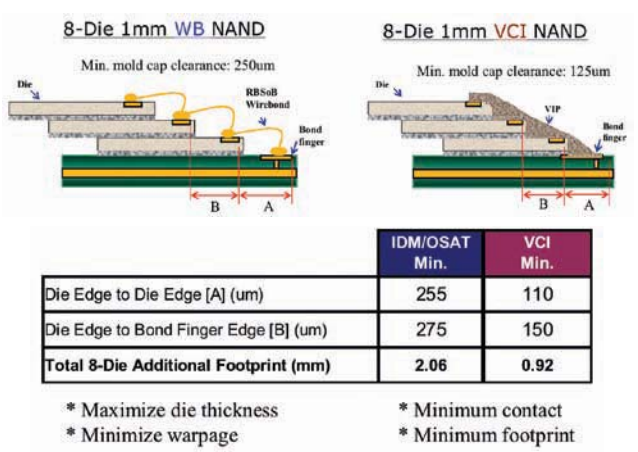


**Figure 3.** Stagger stacking.



| | IDM/OSAT Min. | VCI Min. |
|---|---|---|
| Die Edge to Die Edge [A] (um) | 255 | 110 |
| Die Edge to Bond Finger Edge [B] (um) | 275 | 150 |
| **Total 8-Die Additional Footprint (mm)** | **2.06** | **0.92** |

* Maximize die thickness
* Minimize warpage

* Minimum contact
* Minimum footprint

**Figure 4.** Wire bond and conformal conductor stair step offset stacks.

**Figure 5.** Side view of arrow stack with conformal interconnect.

(**Figure 5**). In some cases, the footprint reduction can provide the critical difference allowing a new, but larger die to be stacked and fit in a standard micro-SD memory card. While most high-volume applications have been for memory die, this approach also works well for mixed die stacking.

## Die Edge Insulation

Forming a conformal conductor on the edge of the die stack requires edge insulation to prevent electrical leakage from the conductor to the die edge. After investigating several glass-like insulations, a thin conformal coating of parylene was found to be an ideal edge insulation for all stacking configurations. With a focus on high-volume manufacturing methods, wafer scale processes were developed that allow parylene to be applied to the die edges prior to die singulation.

In the standard dice-before-grind process, parylene can be deposited on the wafer following the initial, partial cut step, which exposes the die sidewalls. Die singulation occurs after back grind, and a die attach film is applied to the die backside, insulating it and serving as the primary means of attachment from one die to the other. Alternatively, in a grind-before-dice process, the parylene can be applied after the sawing step, while the die are still arrayed on a backing tape.

In some cases, the parylene coating step can be delayed until after the die have been stacked. This is especially useful for the stair-step stacking of flash die because it is a lower cost solution. In this coat-after-stack method, die are offset stacked on substrate strips. Then the whole substrate is placed in the parylene deposition chamber, coating is simultaneously applied to all die in the stack and all die stacks on the substrates, on many substrates. Thus, the economy of scale minimizes the cost of the coating step.

The coating step results in an extremely tough, impervious layer of parylene dielectric insulation over the die pads that must be removed to make an electrical connection to these pads. Laser ablation, using an excimer laser source, resulted in high removal rate selectivity between the parylene and the metal pads, essentially leaving the pads unaffected by the ablation of the parylene. Furthermore, appropriate optics and masks allowed the excimer laser beam to be spread over a wide area so that multiple pads could be ablated simultaneously; key to minimizing the process cost for this step.

For chip scale wafer level packaging flows, ablation can be performed while the die are still arrayed in wafer form. In the case of parylene coating after stacking for offset die, the ablation can be done on multiple die in the stack or multiple stacks on the substrate.

## Vertical Interconnections

Gold wire has been used extensively to connect integrated circuit die to package substrates, and to each other for many years. But gold is very expensive, and numerous efforts are underway to reduce or remove gold from the package assembly bill of materials to reduce package material costs.

The approach discussed in this article for inter-die and die-to-substrate interconnects eliminates the use of gold in the package. Several materials were successfully applied as liquids and then hardened to become solid conductors after appropriate thermal cure cycles. Early successes were achieved with silver-filled epoxy polymers whereby silver particles are held in contact with each other and also against the device contact pad and substrate pads.

More recently, nanoparticle inks were used for products requiring reduced pitch. Some inks were silver based, while others included alternative conducting metal systems. Materials were selected so that cure temperature could be kept low, generally below 200°C, so as not to adversely affect the integrated circuit die.

Numerous application techniques are possible, but the most successful were dispense systems typically used for dispensing flip chip underfill and liquid die attach materials. A pulse dispense, jetting system routinely deposited silver-filled epoxy materials at pitches approaching 200 µm. Newer spray-based systems coupled with advanced nanoparticle materials handled applications requiring conductor pitches below 100 µm.

**Figure 6** depicts 100-µm conductors deposited on the edge of a stair-step stack of flash die at 200-µm pitch. **Figure 7** shows a 16-die stack, and **Figure 8** depicts 30-µm-wide conductors deposited on a test vehicle stack with contacts at 200-µm pitch.

## Electrical Characteristics

While higher in bulk resistivity than gold wire, the larger cross-sectional area and short lengths of the conformal conductors result in resistances in the tens of milliohms, which is quite acceptable for most products. The larger diameter conductors provide lower inductance.

In most applications, both simulations and actual measurements have shown better signal integrity with this construction, resulting in higher operating speeds for speed-critical products such as DRAM.

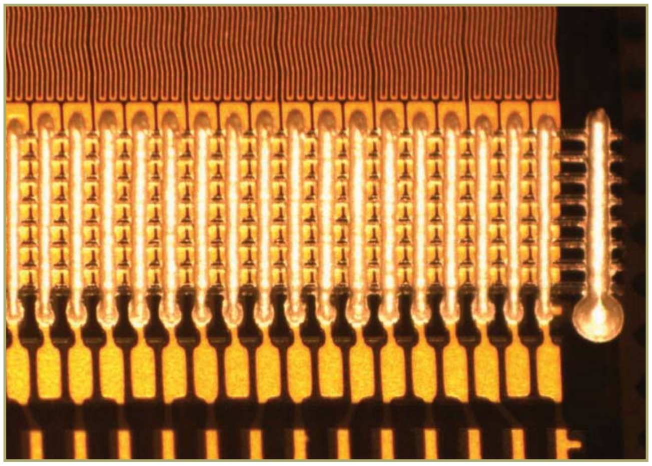


**Figure 6.** 100 µm conformal conductors at 200 µm pitch on 8-die stack.

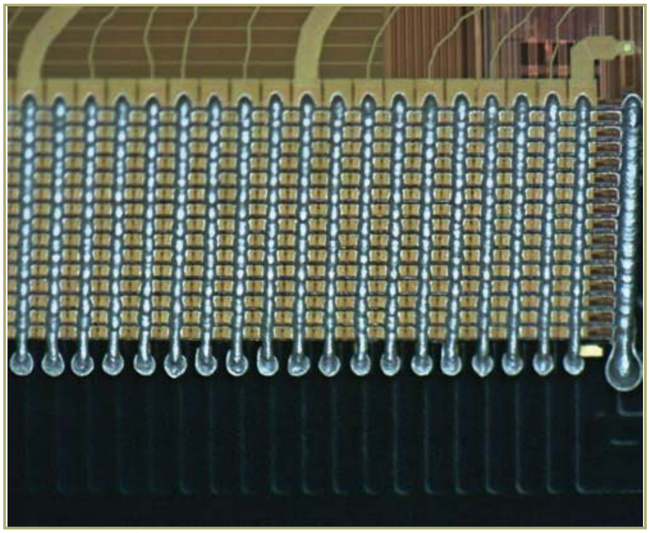


**Figure 7.** 16-die NAND flash terraced stack.

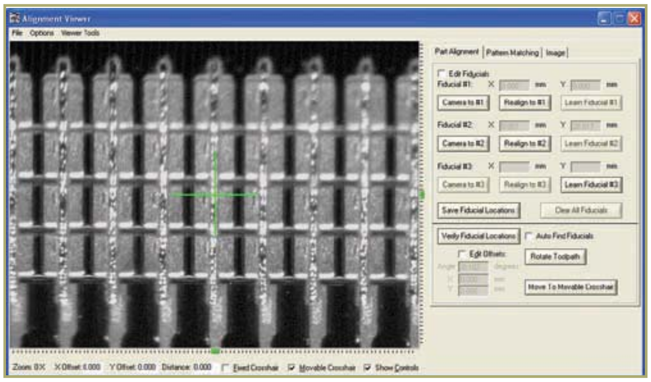


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**Figure 8.** 30 μm conductors at 200 μm pitch on 4-die stack.

## Final Packaging Steps

Once the vertical connections are applied and cured, standard back-end packaging techniques are used to mold the stacked die into standard LGA/BGA, memory card and other appropriate end-product configurations. We worked closely with high-volume licensees to implement 8-die and 16-die flash memory stacks in micro-SD cards for removable memory storage applications, and into molded LGA/BGA packages for solid state drives.

**Figure 9** shows an 8-die flash memory stack on a memory card substrate prior to mold. The technology is also ideal for stacking wafer level flip chip CSP die and leadless QFN packages.

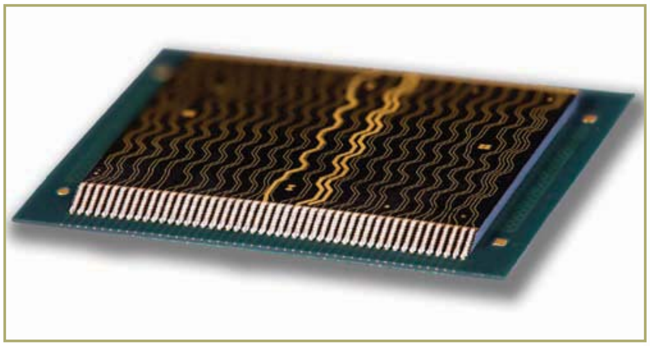

**Figure 9.** 8-Die flash memory stack on substrate prior to molding.

## Conclusion

Mobile internet enabled devices are driving 3D packaging technology solutions. While TSV has much potential, other low cost packaging solutions can also fit in the existing back-end infrastructure.

Using conductive filled polymers and nanoparticle inks, a new interconnect technology replaces wire-bonds and offers smaller footprint, lower cost and high performance. A back-end assembly-based technology was used to implement a wide range of multi-die memory and mixed die components.

Most recently, 32-gigabyte MLC, 12.5 × 15.0 × 1.0 mm ONFI LGA components were qualified using an 8-high tier stack construction, and 64 GB MLC, 14.0 × 18.0 × 1.2 mm ONFI LGA components using 16-high tier stack construction; both based on 34 nm NAND flash die. These are eye-popping capacities in very small form factor packages and clearly illustrate that a low cost back-end 3D implementation can be a very competitive solution for mobile Internet products.

## Acknowledgments

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# NEWS

## Electronic Components and Technology Conference (ECTC), June 1-4 Call for Abstracts

Las Vegas, NV…The **ECTC** Program Committee invites you to submit an abstract for the 60th Electronic Components and Technology Conference (ECTC), to be held June 1 – June 4, 2010, in Las Vegas. This premier international conference is sponsored jointly by the IEEE Components, Packaging and Manufacturing Technology Society (CPMT) and the Electronic Components Association (ECA).

The ECTC comprises papers covering a wide spectrum of topics, including electronic components, ICs, MEMS, materials, assembly, interconnections, packaging, system packaging, optoelectronics, reliability, and simulation. An included emerging technologies program addressws exciting new developments and applications in the area of bioelectronic packaging, flexible/printable electronics, green, and portable power supply packaging. A plenary session and a panel discussion address selected topics each year, in addition to a seminar organized by the IEEE CPMT Society. A focus this year will be to increase the number of papers in new areas of overlap between committees such as opto-interconnect. Authors from companies, research institutes, and universities located around the world presented more than 300 papers and posters at the 2009 ECTC with presenters from approximately 20 countries.

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