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January 2009



- **Cost Reduction of Wafer Level Packaging with TSVs**
- **3D Wafer Level Packages**
- **Innovative Cooling for 3D Die Stack**

Keywords:

side interconnect edge silicon via (ESV), 3D stacked die, 3D WLP, TSV, multichip packages, CIS (CMOS image sensor)



3D Wafer Level Packages for Memory and Image Sensor Applications

A new side interconnect edge silicon via (ESV) uses a conductive filled polymer interconnect for low cost stacked packaging of flash memory, DRAM and CMOS image sensors, adhesive jetting.

By Marc Robinson, Vertical Circuits Inc. [marc.robinson@verticalcircuits.com]

Modern microelectronic technology has greatly enhanced the functionality and complexity of consumer electronic products while simultaneously simplifying their operation for users. The continuing explosion of individual, handheld devices such as cell phones, PDAs, digital cameras and music players, and GPS devices has now become a convergence of these technologies into single, handheld devices that are small, lightweight and inexpensive (Figure 1).

There has always been a dream that all the required functionality for the many functions and features of these devices could be implemented in single chip silicon. However, that dream has not proven to be practical or cost effective. By subdividing complex systems onto separate

chips and targeting each function to the best silicon process for that particular circuit, designers have been able to optimize yields and improve the reliability of their supply chain. Also, when large amounts of memory must be included in a product, multiple chips are often more cost effective and, sometimes, the only possible way to do so.

Sensors have become ubiquitous, with image sensors now included in many converged products. CMOS image sensors are ideal for this purpose because they can be manufactured using standard, CMOS wafer processing techniques, operate at significantly lower power, and can include on chip much of the sensor's required support circuitry.

The inclusion of image sensors (along

with processors, memory, RF and many other chips in small, handheld devices) has driven the development of electronic packaging technologies to deal with the devices' special needs, and to support long-term form factor, functionality and cost roadmaps. As such, there has been much focus on thinning devices, reducing footprints and stacking chips. Wafer level packaging methods have been developed and applied to this problem, with a wide range of complexity and success.

Recently, much has been written about through-silicon via (TSV) methods for packaging CMOS image sensors,¹⁻³ as well as complex wafer level packaging techniques that focus on protecting the image array. But alternative wafer-level packaging technologies exist that have worked well for other chips in converged systems. Wafer-level packaging used to stack memory die can also be adapted to address the unique demands of CMOS image sensors, because many similarities exist in their respective problem sets.⁴

Our packaging development efforts have focused on modifying and optimizing materials and methods for low cost, low temperature stacking of memory die, packaging of CMOS image and other sensors, and integrating sensors with other ICs in multi-die packages. Our methods use wafer-level, thin, conformal, transparent dielectric coatings to insulate the die edges so that conformal conductors can be routed over these edges. These coatings also protect the imaging surface and micro-lens array of CMOS image sensors. By using existing



Figure 1. Consumer product convergence

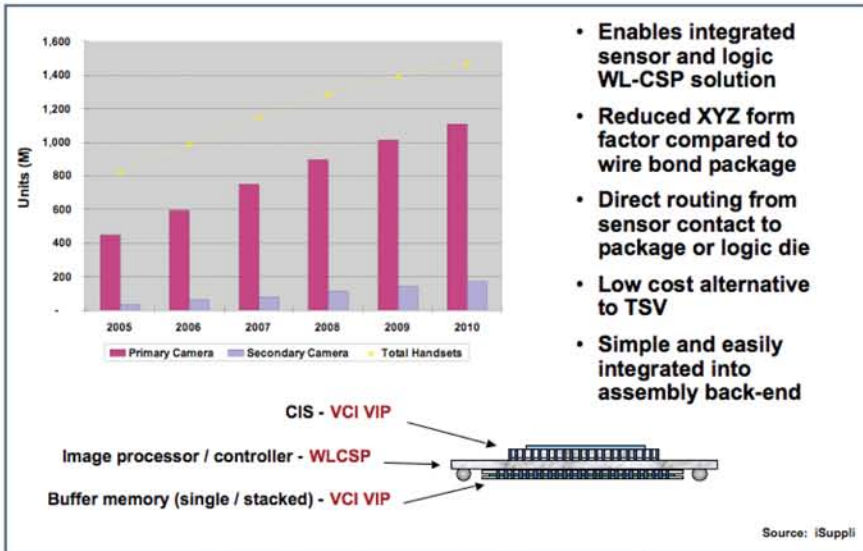


Figure 2. Example cross section of a camera module

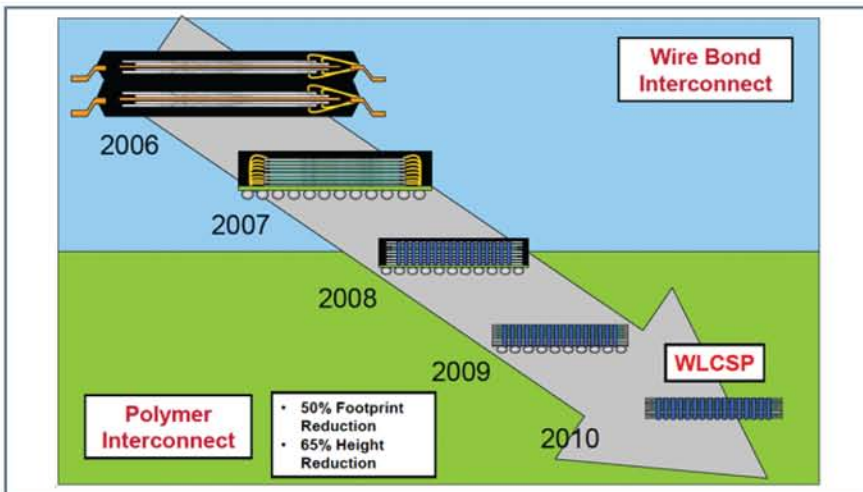


Figure 3. The multichip wirebond to WLP transition

OSAT (Out Sourced Assembly & Test) assembly capabilities, large capital investments for fab-like processing equipment can be avoided.

Memory Stacking

Parylene can be used as a conformal coating and edge insulation on die so that conductors can be formed on the edge of a die stack, without shorting to the silicon die.⁵ Parylene films as thin as 1 μm exhibit dielectric strengths greater than 100 volts, exceeding the requirements of most microelectronic systems, which typically operate at potentials well below 5 volts. Wafer level, high-volume manufacturing techniques compatible with die before- and after-grind processes allow the die sidewalls to be coated with a thin parylene layer at low cost.

For high capacity NAND flash memory cards, the parylene coating is applied to the exposed die surfaces after stacking to further simplify the process and reduce cost. A conducting silver-filled liquid is applied to the edge of a die stack to form inter-die connections. Then the stack is cured at a low temperature to solidify the conductor into a glass-like inter-die electrical connection.

Using mainstream assembly equipment for dispensing liquid epoxies, high-speed hybrid jetting techniques apply the inter-die conductors to the die stack sides and connect the die to the package substrate. Figures 4 and 5 show a 16GB memory card formed by stacking 8 die insulated and interconnected in this manner. Figure 6 depicts the process flow used to make the cards.

Various conductive pastes can be used, many of which contain epoxy binder resins and are highly filled (>80% w/w) with silver particles. Maximum particle size must not exceed 50 μm to prevent needle clogging, obtain fine line widths and minimize pitch between lines. Paste viscosity can vary between 20-80KcP. Specific cure cycles are followed and kept below 180°C, which minimizes any thermal effects on the memory die.

Material properties can be manipulated to manage interactions between the paste, deposition equipment and substrate, such as slumping and wetting phenomena or interfacial adhesion through optimization of cure temperature and time. We have had the best success in controlling the size and shape of interconnects, and meeting high volume throughput requirements by using a hybrid dispense method with the volumetric accuracy of jetting and the positional accuracy and material control of needle dispensing.

Following polymer interconnection, the substrate strips with attached and interconnected die stacks are molded using standard IC package molding equipment and methods. Because of the small footprints, die that are too big to package by wire bonding can fit in standard format memory cards.

Electrical properties have been well studied and are quite adequate for the short interconnect distances between the die, exhibiting resistances in the tens of milliohms.

Product reliability with this technique has been well characterized and meets the

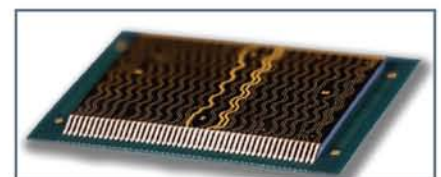


Figure 4. Inter-Die Edge Connections

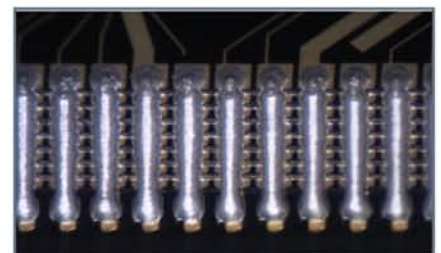


Figure 5. Close-up view of inter-die edge conductors

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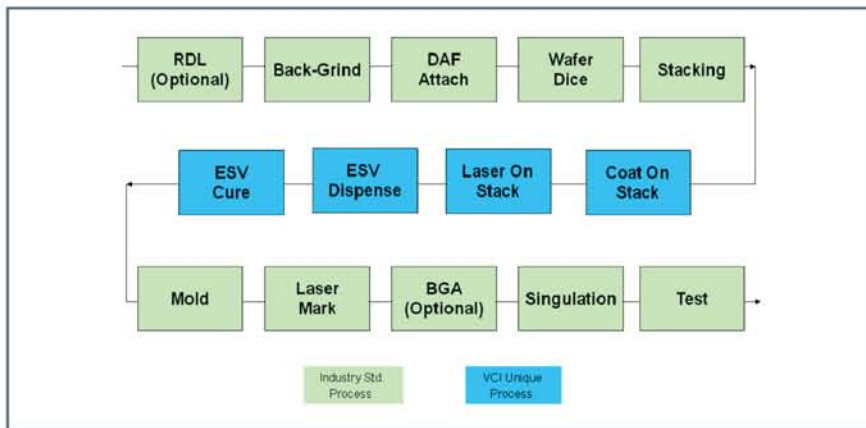


Figure 6. Edge Silicon Via Process for Flash

stringent requirements for server DRAM modules, far exceeding the needs of consumer memory products.

With ESV packaging, inter-die connections in contact with the die edge result in small component footprints barely larger than the die. The ESV interconnects are as close as you can get to TSV, without needing any vias in the die. A non-disruptive approach, side interconnect stacking technology can use today's extensive back-end infrastructure for low cost, high volume manufacture.⁶

CMOS Image Sensors

Image sensor packaging requirements sound simple, but are in fact difficult to achieve. Primarily, the sensor must remain unobscured by the package and protected from damage during manufacturing and throughout the in-service life of the product into which it is incorporated. Because the connection pads are on the chip's image sensor side, a means must be provided to move the signals from the front surface to the back for connection to a circuit board.

Micro-lenses on the chip's surface for improving light sensitivity, as well as the RGB filter coatings on the sensor's surface, are usually fabricated from polymers that cure at relatively low temperatures. They can be deformed or damaged by excessive processing temperatures during packaging. So to avoid such damage, low process temperatures must be used during packaging. Obviously, any coatings placed over the imaging area must be optically compatible.

To address these requirements, image sensors can be mounted in a cavity package using wirebonds and a cover glass for protection and optical access to the sensing array. This increases the sensor's thickness and footprint above what would be required for a chip-scale approach. Others have been successful with a wafer level packaging approach or with TSV techniques^{7,8} to get the signal from the front side to the back without increasing the footprint. Essentially a front-end solution, TSV requires expensive equipment, and much process development, before it can be considered ready for reliable, low cost manufacture.⁹ Al-

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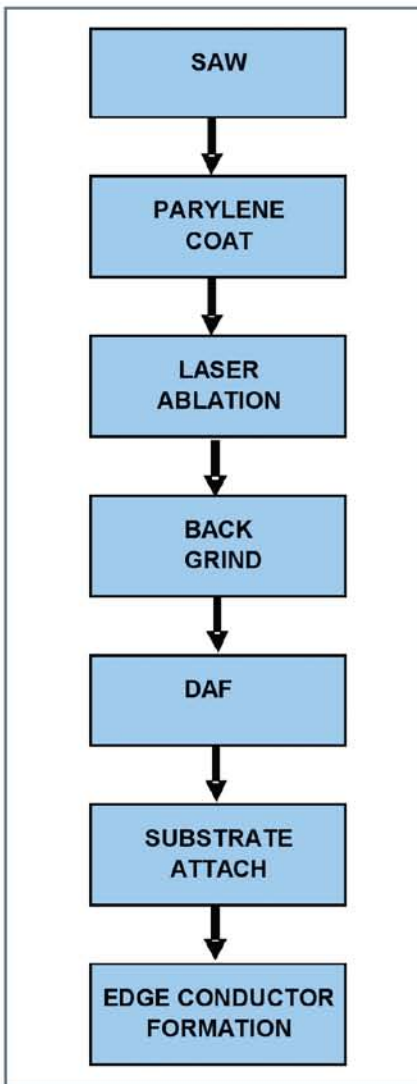


Figure 7. Process flow

though successful at minimizing footprint, the capital equipment costs and lack of process maturity are obstacles to widespread adoption of TSV.

Polymer Interconnect Method For CIS

Figure 7 depicts the basic process for the low cost, assembly-based image process package. First, the CMOS image sensor wafers are sawed. For thin die processing and handling, the saw height is set to a value slightly deeper than the final die thickness, but not deep enough to fully singulate the die.

The wafers are then placed in a parylene deposition chamber, and a thin coating is deposited at room temperature on the front surface of the image sensor die and on the exposed die edges. The coating forms a

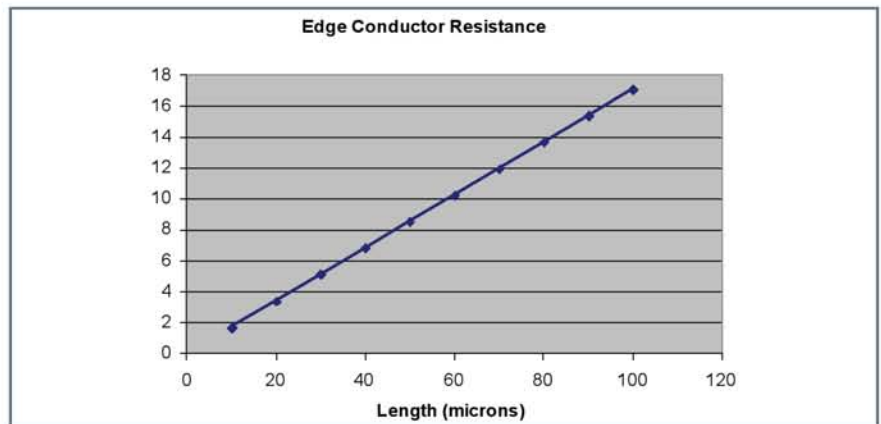


Figure 8. Edge interconnect resistance

super thin pinhole-free layer that puts zero stress on the sensor because it exhibits no CTE shrink during cure. Also, there is zero particle damage risk during processing, and the coating is optically neutral.¹⁰ It also protects the wafer during processing instead of the glass and other substrates needed by TSV and other well-known wafer scale packaging methods. We have experimented with coating thicknesses in the range of 1 to 5 microns, but thinner coatings are possible.

A laser ablation system removes the deposited coating from the connection pads on the die's front surface. Parylene is transparent in the visible range between 300 and 800 nanometers, so a short wavelength must be chosen to promote sufficient energy absorption in the coating layer for ablation to occur.

The wafers are then back-ground, typically leaving a die thickness of 50um or less and singulating the die. An attach film can be applied to the die while they are still in wafer form. The singulated die are then attached to an appropriate substrate, circuit board or another die.

Forming virtual conductive vias, high speed hybrid jetting techniques apply a silver-filled conductive liquid to the side of the die that connects the pads on the front with the underlying substrate or die the sensor is mounted on. As the conductors are formed on the die edges, the package footprint is very similar to that of a TSV, but much smaller than wire bonds. In addition,

this method can also mount die directly on system circuit boards and flex cables, further reducing the profile of handheld systems.¹¹

Resistances for edge conductors formed by this method are shown in Figure 8. For a die thickness of 50 microns, a connection resistance of less than 10 milliohms was observed.

The parylene was deposited at room temperature, and other process temperatures for this packaging method do not exceed 160°C. So the micro-lenses do not flow or deform. While a glass cover slide can still be incorporated in the package if required, our experience indicates that the parylene coating provides sufficient protection to the image sensor surface for most consumer applications.

Package Flexibility

The final package can consist of a single image sensor mounted on a substrate, or the image sensor can be incorporated with other die in a multi-die package. Figure 9 depicts a single image sensor mounted on a BGA substrate, while Figure 10 shows a multi-die package consisting of an image surface integrated with an image processor and a stack of

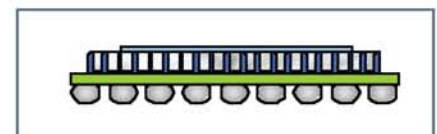


Figure 9. Polymer interconnect CIS package



Figure 10. Polymer interconnect multi-die package

memory die underneath. In both cases, the die are edge insulated with parylene and conductive epoxy is used for inter-die and die-to-substrate connections.

Conclusion

The low temperature application of parylene as an edge dielectric, and the use of conductive filled plastic materials for die interconnection result in a low temperature, low cost, high-volume manufactur-

ing process for multiple die memory stacks, or single die such as CMOS image sensors that require connection from the back. Implementation of the process in OSAT assembly facilities uses existing assembly equipment, thereby easing adoption and minimizing capital costs. In summary, this method can successfully stack memory die and has been adapted for the packaging of CMOS image sensors.

Notes

1. This article is based upon the paper "3D Wafer Level Packaging Technology For CIS Applications" presented at the 5th Annual International Wafer Level Packaging Conference, Oct. 13-16, 2008, San Jose, CA. ©SMTA.
2. The processes described in this article are the subject matter of a number of granted and pending patents. Vertical Circuits offers licenses for this technology. Call 1-831-438-3887 or www.verticalcircuits.com for more information.

Acknowledgements

The support of key equipment and material suppliers Asymtek, DISCO Corporation, LORD Corporation, Resonetics, and Specialty Coating Systems is greatly appreciated, as are the efforts of the team at VCI.

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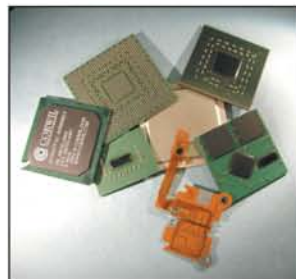
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