



Vertical Circuits Inc



Confidential

Vertical Circuits Inc. NAND Flash Product Qualification

DOC1122-00

REV A

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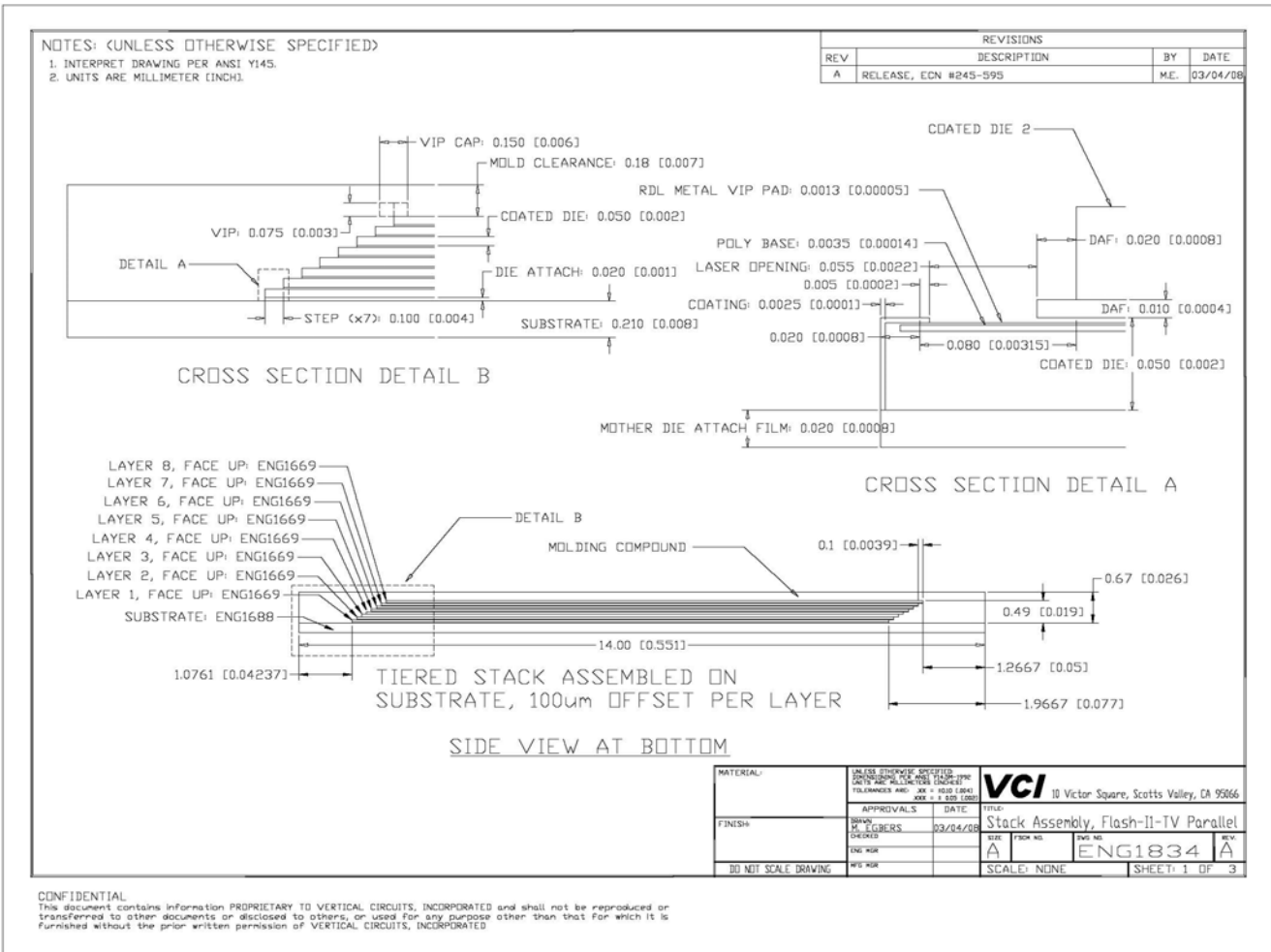
1.0 PURPOSE

1.1 The purpose of this document is to present the reliability/qualification requirements, procedure and results for Vertical Circuits Inc. NAND Flash packaging technology.

2.0 SCOPE

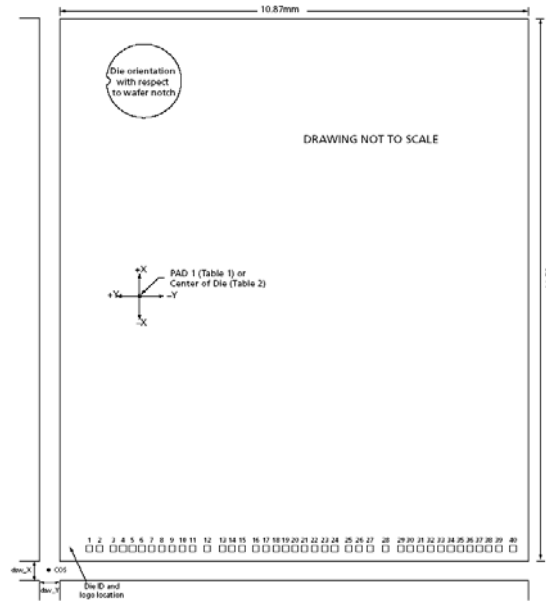
2.1 This Vertical Circuits NAND Flash Product qualification report (VCI.DOC1122) presents the reliability testing and product qualification procedures and data for stacked NAND Flash die in component form. The components are packaged in a plastic Land Grid Array format, and employ the Open NAND Flash Interface (ONFI) pad/ball assignment. This document serves as the qualification envelope specification for similar/derivative NAND Flash products.

2.2 Primary Qualification Vehicle: 0.9x14x18mm LGA, 8 x L41b 8Gb NAND (14.52x10.87mm):

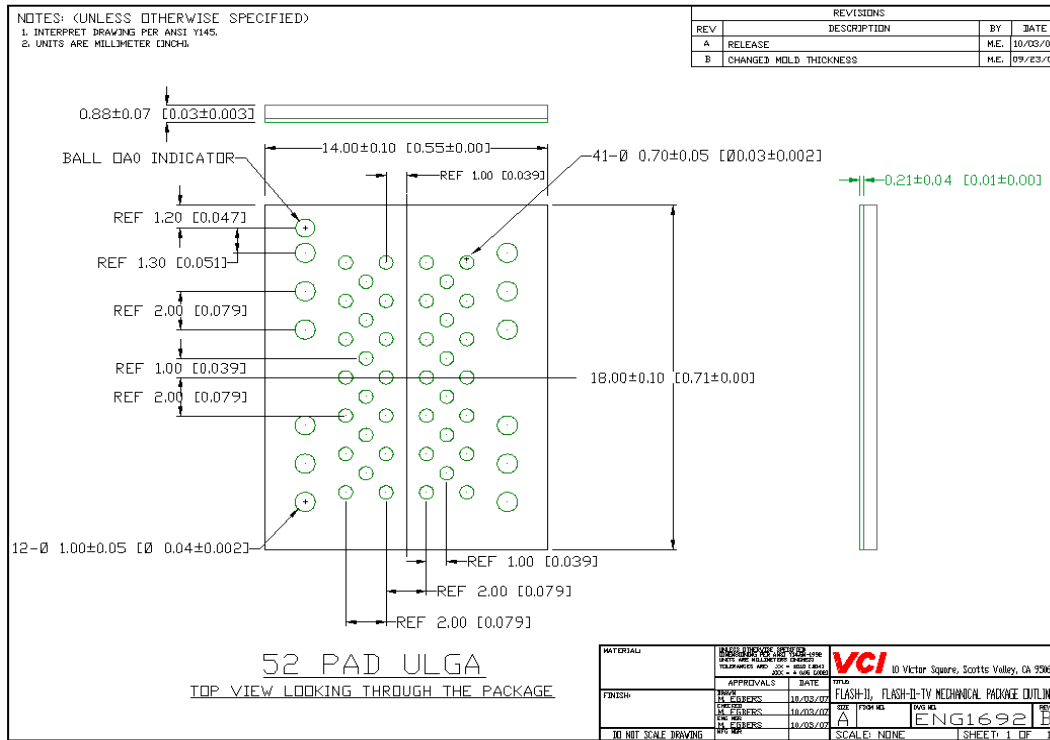


3.0 SILICON DEFINITION

3.1 L41b: 8Gb x8/16 NAND Flash (200 & 300mm), MT29F8G08MAA. For product datasheet, refer to: www.micron.com/products/nand.



4.0 PACKAGE PIN-OUT DEFINITION



5.0 BILL OF MATERIALS AND PACKAGE CONSTRUCTION

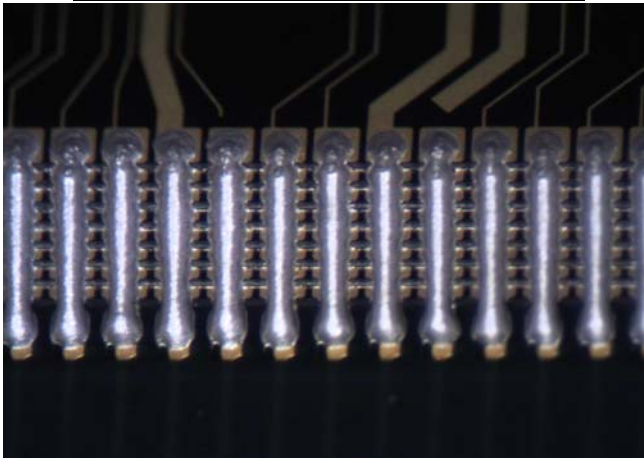
5.1 Bill of materials:

ITEM	MATERIAL	SPECIFICATION
Silicon IC	L41b 8Gb NAND	90x90um Native Pad (Al)
Redistribution Layer	Polyimide* (PW1500)	3.0um PI, 1.5um Au, 0.3um TiW
Coating	Parylene-C	2.5um final coating thickness
Die Attach Film (Mother)	Hitachi FH-900	20um incoming film thickness
Die Attach Film (Daughter)	Hitachi FH-900 or Nitto EM-500	10um incoming film thickness
Epoxy Mold Compound	Nitto GE100LFCS	175um clearance from top die
Vertical Interconnect	Lord MD-141	200um line on 110um tier

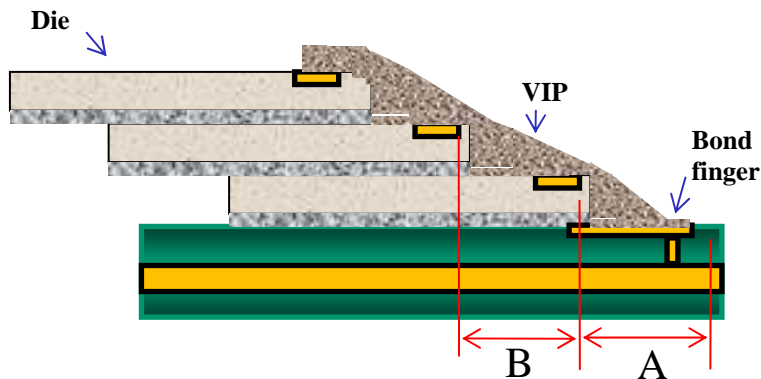
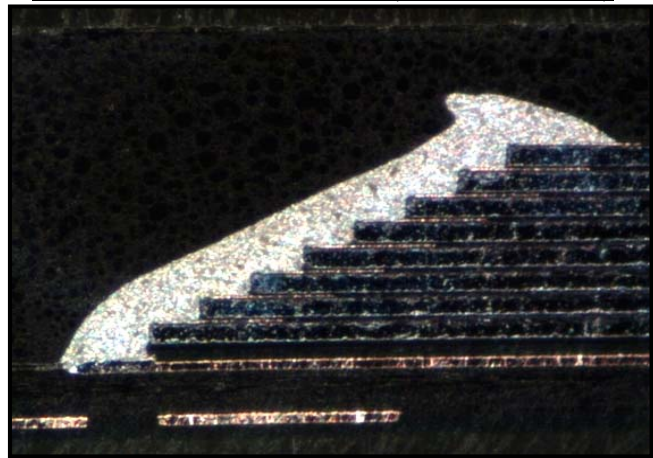
* Native wafer polyimide may be used.

5.2 Package construction:

Vertical Interconnect Pillar: Front View



Vertical Interconnect Pillar (C/Section View)



B=0.11mm, A=0.15mm

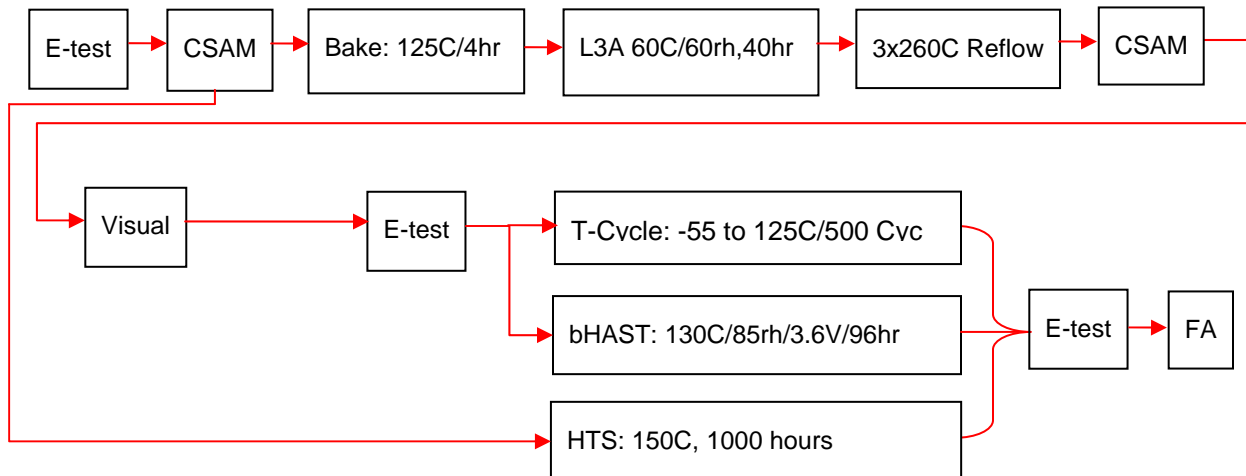
6.0 QUALIFICATION ENVELOPE

6.1 The following product characteristics and dimensions define the qualification envelope:

Feature	Nominal	Maximum
# Die	8	
Stack Type	Tier-Offset	
Package X	14.0mm	14.1mm
Package Y	18.0mm	18.1mm
Package Z	0.88mm	0.91mm
Pakage Warp		0.060mm
PCB Z	0.210mm	0.230mm
EMC Z	0.670mm	0.680mm
DAF Z (Die-0)	0.020mm	0.023mm
DAF Z (Die 1-7)	0.010mm	0.012mm
Die-X	10.87mm	10.9mm
Die-Y	14.52mm	14.6mm
Die Z	0.050mm	0.053mm

7.0 RELIABILTY TEST PROCEDURE AND SPECIFICATIONS

7.1 The product, once completed assembly, is subjected to the following test procedure. JEDEC test specifications are followed in all procedures. Additional Smart Digital card-level mechanical tests are also performed.



Additional Mechanical Tests:

- Drop Test, 1.5m.
- Bend Test, 10N.
- Torsion Test, 10NM.

8.0 ASSEMBLY WORKMANSHIP DATA

8.1 Lot loading and assembly electrical yield:

	Assembly Lot#	Process Flow	Assembly Yield*	Assembly Completion
L41 TV	ENG2008-194A	Coat After Stack	100%	22-Aug
	ENG2008-189B/C	Coat After Stack	96%	22-Aug
	ENG2008-187A	Wafer DBG	100%	22-Aug
L41 LIVE	ENG2008-205A	Coat After Stack	82%	31-Aug
	ENG2008-152A/B	Coat After Stack	79%	22-Aug
	ENG2008-186A	Wafer DBG	84%	22-Aug

***Live 8-High Builds are Subject to the following wafer probe (KGD) testing:**

- Opens/shorts • Input/output leakage tests • ICC standby • Voltage regulator performance
- Nominal VCC functional • LOW/HIGH VCC margin • Memory array algorithmic patterns
- High-voltage stress • PROGRAM performance • ERASE performance • Bad-block marking

Repairs are implemented at each repair test. Repairable die are processed through repair algorithms based on the repair solutions defined during the tests described above. Post-repair testing is conducted with appropriate guard-bands to ensure a consistently high quality level.

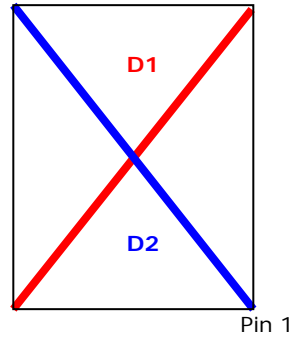
8.2 Assembly visual and dimensional yield data:

8.3 RESULT: 72/72 Units Sampled PASS.

#	Requirement	Baseline Live		Baseline TV	
		Results	Remarks	Results	Remarks
1	Dimensions XYZ	0/72	Passed	0/72	Passed
2	Warpage <60um	0/72	Passed	0/72	Passed
3	Mold Voids - reject if =>10mils	0/72	Passed	0/72	Passed
4	Pin Hole - reject if =>50x50mils	0/72	Passed	0/72	Passed
5	Pitted Surface - reject if =>20x20mils	0/72	Passed	0/72	Passed
6	Mold Flash / Bleed Out	Acceptable	Passed	Acceptable	Passed
7	Incomplete Fill	0/72	Passed	0/72	Passed
8	Crack Package / Micro Gap	0/72	Passed	0/72	Passed
9	Scratch	0/72	Passed	0/72	Passed
10	Discoloration/ Contam/ Foreign Material	0/72	Passed	0/72	Passed
11	Bubble / Blister	0/72	Passed	0/72	Passed
12	Misalign Mold	0/72	Passed	0/72	Passed
13	Popcorn / Substrate Delamination	0/72	Passed	0/72	Passed
14	Chipout	0/72	Passed	0/72	Passed
15	Surface Irregularity	0/72	Passed	0/72	Passed

8.4 Package warpage data:

After PMC (GE100LFCS)			
Unit#	D1 (um)	D2 (um)	Max Value (um)
1	10.09	13.40	13.40
2	21.85	22.26	22.26
3	22.68	17.60	22.68
4	9.89	14.26	14.26
5	13.87	14.30	14.30
6	22.13	21.10	22.13
7	21.92	23.17	23.17
8	21.55	24.19	24.19
9	26.88	30.34	30.34
10	13.28	15.31	15.31
11	17.02	16.53	17.02
12	20.02	20.30	20.30
13	14.41	14.94	14.94
14	21.46	19.85	21.46
	Min	13.40	
	Max	30.34	
	Ave	19.70	
	StDev	4.94	

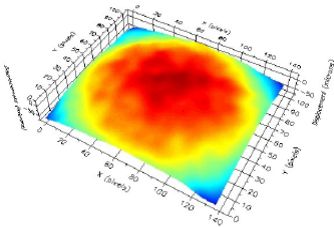


- Warpage measuring equipment:
- Ambios stylus profiler
- Scan set-up:
- Stylus force: 10mg
 - Range: 400um
 - Filter level: 1 (9251 data pt.)
 - Length: 22mm
 - Speed: 2 mm/sec

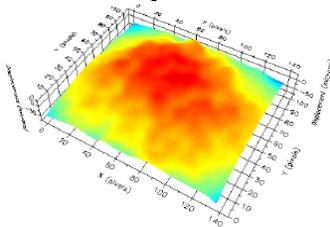
8.5 Shadow Moiré warpage vs. temperature characteristic.

Temperature (°C)	Min Deflect (um)	Max. Deflect (um)	Coplanarity (um)
-55	-58	26	84
-40	-60	23	83
25	-41	21	62
100	-24	11	35
175	-14	8	22
260	-20	16	36

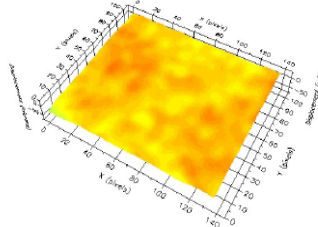
T = -55°C Initial



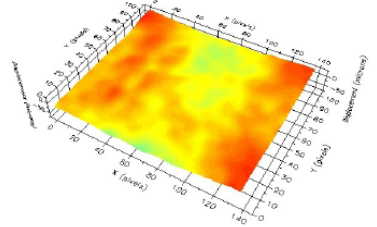
T = 25°C Heating



T = 175°C Heating



T = 260°C Final

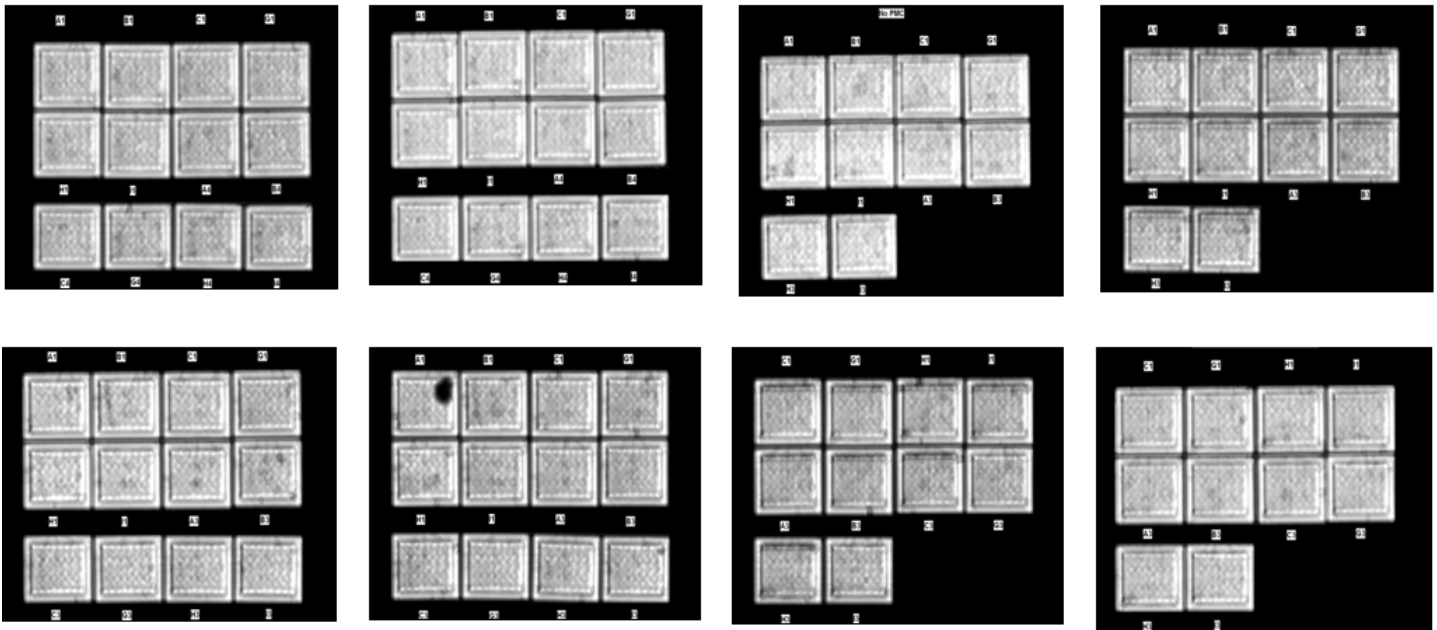


Note: the silicon to package ratio for the qualification vehicle is ~30%. The warpage characteristics above are typical of standard stacked die packages, however, average warpage is minimized by the inclusion of the die coating.

9. MOISTURE RESISTANCE TESTING (PRE-CONDITIONING)

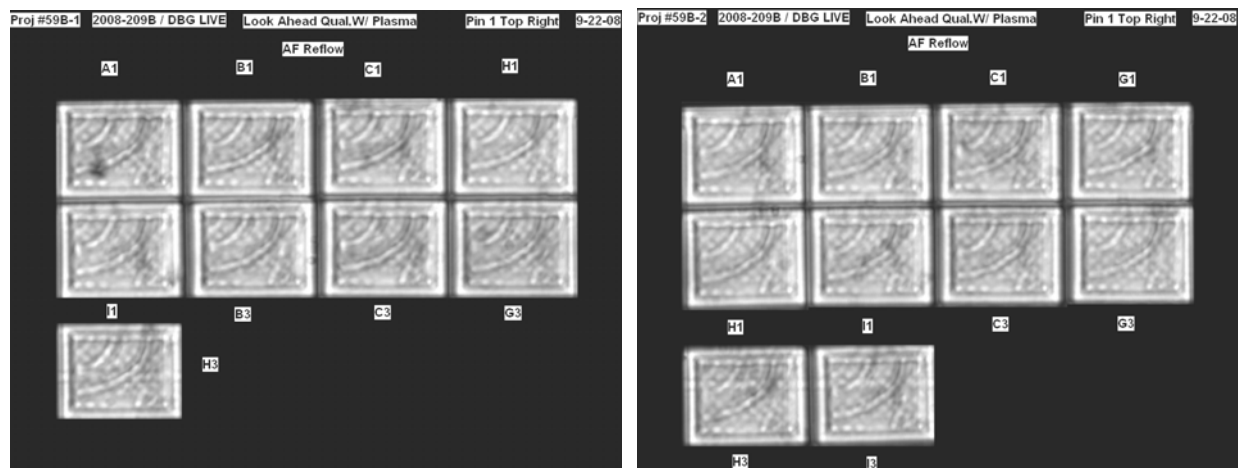
9.1 Scanning Acoustic Microscopy images shown after JEDEC Level 3 preconditioning (including 3 x 260C reflow).

9.2 RESULT: 88/88 Units PASS.



Note: Unit #37 Determined to have a DAF void. This did not grow by >10% or break-out after reflow. All above units use Hitachi FH-900 series DAF (20um Die-0, 10um Die-1).

9.3 Alternate Material Set (Nitto EM-500). In order to improve die-attach yield on thin live die (die pick-up yield), Nitto EM-500 is also a recommended and qualified material for die to die bonding. Pre-plasma is necessary for EM-500.



Note: Nitto EM-500 10um die-to-die bonding on live L41 die. Images after MRT.

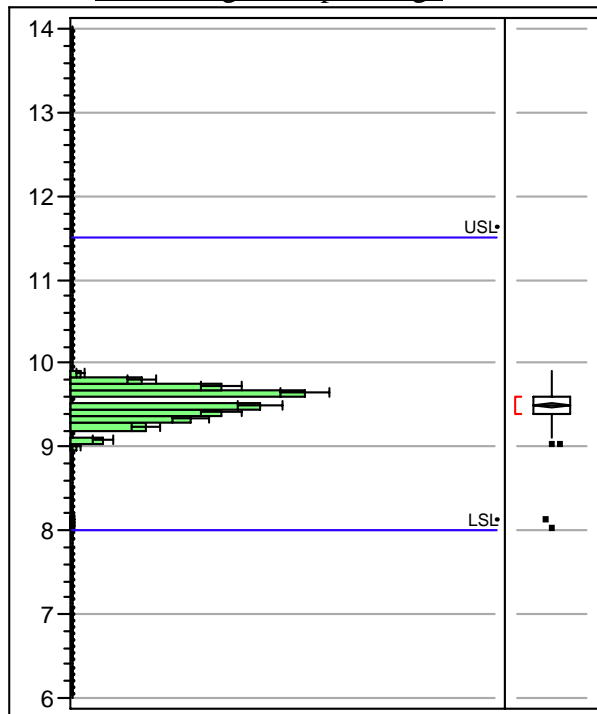
10. HIGH TEMPERATURE STORAGE

10.1 High Temperature Storage is performed at 150C in a purged Nitrogen oven (JEDEC condition B). 3x15 samples (45 units) submitted for testing. Before and after results are tracked on a per unit, per die and per net basis

RESULT: 45/45 Units PASS.

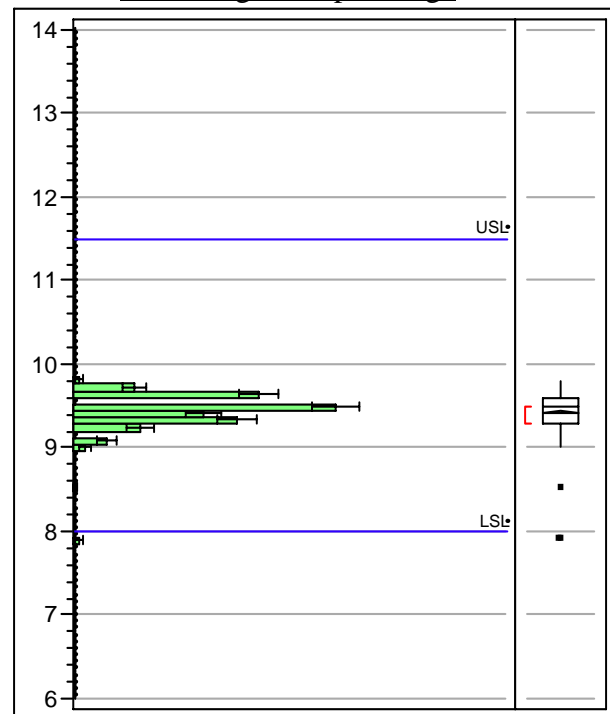
	T-Zero.Resistance	HTS.Resistance	HTS.Resist.Delta
MEAN	9.49	9.43	-0.7%
ST.DEV	0.22	0.21	1.2%
MIN	8.00	7.90	-9.4%
MAX	9.90	9.80	2.2%
RANGE	1.90	1.90	11.6%

Before High Temp Storage



CpK = 2.77

After High Temp Storage



CpK=2.24

Note: silver-filled polymers will shrink slightly over time creating greater particle to particle contact, and hence thermal processes including storage will tend to improve (lower) resistance slightly as above.



11. MECHANICAL DROP, BEND AND TORSION TESTING

11.1 Mechanical drop test, bend test and torsion tests (twist test) were performed on completed devices.
RESULT: 45 Units PASS.

11.2 Drop Test:

- 11.2.1 Equipment: Accu Drop 160.
- 11.2.2 Specifications: 1.5m, 1G, 30 Cycles.
- 11.2.3 Temp = 23C, RH=55%.
- 11.2.4 15/15 pass (2 separate runs).

11.3 Bend Test:

- 11.3.1 Equipment: SE 1220S (Load Cell AL-50K).
- 11.3.2 Specifications: 10N Force (both sides), 5 cycle, 60s hold.
- 11.3.3 Temp = 23C, RH=55%.
- 11.3.4 15/15 pass (2 separate runs).

11.4 Torsion Test:

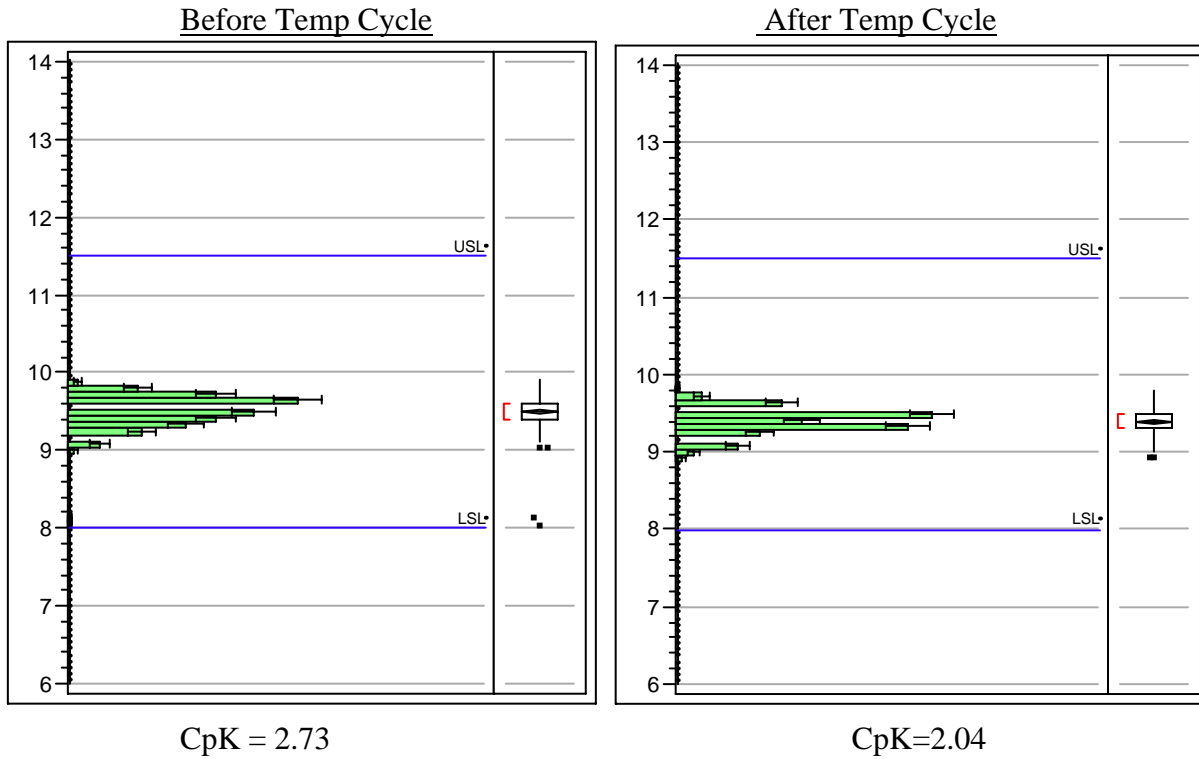
- 11.4.1 Equipment: 2205S.
- 11.4.2 Specifications: 10 Nm, clock/counter-clock 5 times each.
- 11.4.3 Temp = 23C, RH=55%.
- 11.4.4 15/15 pass (2 separate runs).

12. TEMPERATURE CYCLING

12.1 Temperature cycling from -55C to 125C (JEDEC condition B) was applied to units with pre-conditioning (JEDEC solderable component specification) and without preconditioning (SDI car specification).

12.2 **RESULT: 77/77 Units PASS (45/32 Preconditioning Split).**

	T-Zero.Resistance	MRT.Resistance	MRT.Resist.Delta	TC500.Resistance	TC500.Resist.Delta
MEAN	9.48	9.43	-0.7%	9.41	-0.6%
ST.DEV	0.21	0.21	1.2%	0.16	1.8%
MIN	8.10	8.10	-9.4%	9.00	-6.5%
MAX	9.90	9.84	2.2%	9.80	9.4%
RANGE	1.80	1.74	11.6%	0.80	15.8%



Note: it is recommended for temp cycle reliability on structures requiring an interconnect span greater than 12.5mm in length, that mechanical vertical interconnect structures are included as the outer two columns.

13. BIASED HAST TESTING

- 13.1 Biased High Accelerated Age Testing is performed at 130C, 85% RH, and at 3.6V DC. Alternating +/- biased is applied to nets where applicable. The test is performed for 96 hours with continuous readout on DC amps/volts.
- 13.2 **RESULT: 60/60 Units PASS (20 L41b, 40 L41 TV).**



14. CONCLUSIONS

14.1 Vertical Circuits' NAND Flash products are compliant with JEDEC Component and SDI Memory Card qualification specifications under the following conditions:

TEST	CONDITION	S.S.	RESULT
Moisture Resistance Testing	L3 Soak, 3x 260C Reflow	88/88	PASS
High Temperature Storage	500 hours (B)	45/45	PASS
Temperature Cycling	-55 to 125C (B), 500 cycles	77/77	PASS
Biased HAST	130C/85%RH, 3.6V, 96 hours	60/60	PASS
Drop, Bend, Twist	1.5m, 10N, 10Nm	45/45	PASS

14.2 All units were constructed using qualified and automated high-volume manufacturing equipment.

14.3 The qualification envelope includes all existing Vertical Circuits' NAND Flash assembly flows (*Coat After Stack* and *Wafer DBG*), package body sizes of up to 14x18mm and down to 0.8mm thickness, die sizes of up to 12x15mm, and die thicknesses of greater than 0.040mm.