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COVER STORY

How 3D is Stacking Up

BY GEORGE A RILEY, PH.D, *Contributing Editor*

Through-silicon vias (TSV) have captured the 3D packaging spotlight, as evidenced by crowded conference sessions, a tsunami of technical papers, and an increasing buzz about how great it's going to be — when they finally do it. Attracted by the growing demand for higher performance in less space, more than 50 companies are reportedly progressing towards commercializing TSV. The eventual winners must find paths that include acceptable prices, scalability, established supply chains, and commercial payoffs large enough to justify their investments.

> THE SHORT STORY ■ While moving towards tomorrow's high-performance 3D packages with through-silicon vias (TSV) has captured most of the attention in the industry, stacked packages and similar established approaches have many 3D advantages and are making substantial, if quieter, technical and market progress.

Meanwhile, in the shadow of this Tower of Babbling, 3D components continue to be produced in high volume by other methods. The producers are making quieter but steady progress to improve and extend the capabilities of proven 3D approaches, or even to introduce new, potentially disruptive ones.

Stacked Die

Die stacking, perhaps the simplest and most used 3D technology, piles up and connects a stack of die. Last year, **Samsung** demonstrated a stack of 16 wire-bonded NAND flash memory die in a single 1.4mm-thick package, using die thinned to 30µm with 20µm adhesive layers. Samsung developed new processes for the 16-die stack, including a new laser-cutting technology to dice the thin wafer, and a method to maintain uniformity of the thin adhesive layer. While Samsung projected no immediate commercial demand for 16-die stacks, they will use these developments to create thinner packaging for their current die stacks.

Edge bonding by creating vertical conductive tracks across the edges of the die stack is an alternative to traditional wire bonding. Edge bonding avoids the complexity of wire bonding and reduces the stack footprint, while eliminating wire parasitics that limit speed and performance.

Vertical Circuits, a technology development and licensing company, introduced high-speed jetting of conductive polymers to create stack edge bonding. The process first redistributes bond pads to the periphery of the die if needed. Die are then coated with a thin dielectric layer that insulates the edges and bond pads. The die are prepared for stack interconnection by removing the insulation from only the bond pads that will be interconnected using laser ablation.

An adhesive binds the die in a parallel or offset die stack. Edge interconnections are made by high-speed dispensing of silver-filled conductive polymer to form a conductive pillar from each exposed bond pad to the bottom of the stack. The conducting columns extend below the bottom die, creating a complete chip-scale packaged stack, ready for mounting on a board, substrate, or in a package.

Figure 1 shows an offset stack of eight die, each about 40µm thick, separated by 10µm thick die-attach film. They are connected to each other and to the substrate by the conductive polymer columns. The horizontal offset for conductive adhesive interconnections is only about 1/3 of that required for wire bonding.

For high-volume manufacturing, the stacks are mounted in a large array on the un-singulated substrate panel before connecting the stacked die to each other and to the substrate. Individual memory cards are singulated from the panel after molding or encapsulation. Eight die are stacked in an 0.8mm total height FBGA package only slightly larger than the die in X and Y dimensions.

Die preparation is at the wafer level. All handling and processing beyond wa-

fer level uses gang or array methods to maximize throughput and minimize cost. Parallel processing, and using silver conductors instead of gold wires, results in lower pricing than for competitive wire-bonded stacks.

No unusual facilitation or assembly equipment is needed, so the capital investment is small.

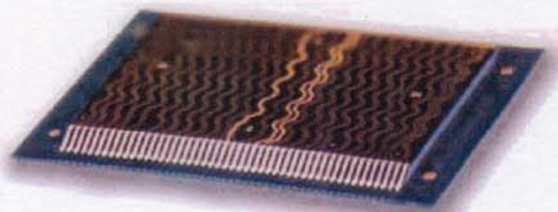

FIGURE 1. Eight die offset stack with conductive polymer interconnections. *Courtesy of Vertical Circuits, Inc.*

Next Generation PoP

Package-on-package (PoP) interconnects stack packages rather than bare die, allowing an easy mixture of die types and technologies, such as memory with control electronics. Packaged components have several advantages over die. Packages are easier to handle, fully testable before assembly, and have established supply chains. However, present stacked packages cannot meet the next-generation requirements for high-density packaging, which are being driven by telephone handset needs such as reduced size, increased pin counts at finer pitch, wider memory bus, dual-channel architecture, and integrated decoupling capacitors.

Last year, **Tessera** developed a copper inter-package contact layer to reduce total stack height in PoP stacking. The contacts are tapered copper micro-pillars with a height of 25 to 175µm, a base diameter of 65 to 375µm, and tip diameter of 40 to 200µm, resulting in lower height and either finer interconnect pitch or wider trace space than conventional CSP solder ball allows.

Amkor is qualifying a PoP approach that meets both present and next-generation needs of smart phones and other high-performance memory applications. Amkor's unique solderable through-mold via interconnections (see AP January 2008) provide a finer pitch, higher density interface between stacked packages. The bottom package supports diverse processor device requirements, as well as providing space for integrated passive components to improve signal quality. The high-density memory interface scales with memory architectures, without changing the SMT PoP stacking process. The bottom package platform allows wire bonded, flip chip, or stacked die configurations. PoP supply versatility provides simplified logistics.

As shown in Figure 2, through-mold vias (TMVs) are cylindrical, solder-filled, fine-pitch vias extending from the top surface of the bottom package to the interconnection layer. Laser ablation creates tapered through-mold openings for the stacked interface. The vias are partially solder-filled, with the mold material separating and defining the vias, permitting finer pitch without short circuits. In attaching the upper package, the BGA solder balls of the top package rest inside the vias of the bottom-package, and make contact with the solder in the vias. Reflowing creates solder columns, surrounded by the mold material providing a mechanically robust interconnect.

Comparison tests between a new structure 14×14mm test vehicle and a similar package in current technology showed that the new structure gives better warpage control, permitting thinner core substrates. Board-level reliability testing of the new package shows significantly better results in thermal cycle, bend tests, and drop tests.

Multilayer Embedded Chips

The recent SMTAI Emerging Technologies session showed that embedded chip packages can sequentially stack multiple layers with many components in each layer. **Fraunhofer IZM** reported that its chip-in-polymer (CiP) approach allows a very high degree of miniaturization. The short, well-controlled interconnections, combined with suitable RF materials, greatly improved high-frequency performance. The demonstration device is a two-layer 77GHz embedded radar module for automotive adaptive cruise controls. Fraunhofer is moving ahead to develop more multi-layer multi-die packages with its technology.

General Electric, proponents of this "chips first" approach since the early 1990's, have kept it alive and improving until the market need for thin stacked die finally developed. In the latest version, also reported at SMTAI, the GE Embedded Chip Build Up (ECBU) solderless process demonstrated high performance capability with advanced copper / low-*k* devices. GE sees applications in high density arrays, where bump size and pitch, power, and metal migration limit of solder bump flip chip connections.

Disruptive New Processes

The Occam process introduced last year by **Verdant Electronics** is a bold attempt to redefine electronics packaging with a built-up multilayer structure of packaged components directly interconnected with plated copper circuits. This eliminates several packaging nuisances, including fine-pitch solder paste printing, lead-free solder, reflow ovens, the handling and testing of bare die, and the nagging concerns of post-assembly cleaning. While Occam's impact will extend far beyond 3D stacking, Occam does accommodate multiple layers of packaged die with other components, and thus 3D. The TPL Group is currently exploring the steps required to commercialize Occam.

FIGURE 2. Cross-section of joined top and bottom packages, showing through-mold vias as gray columns. *Courtesy of Amkor*

The most recent 3D process, 3D silicon, was jointly announced on August 11th by **BeSang, Inc.**, South Korea's National Nanofab Center, and Stanford University Nanofab Center. This process creates a layer of active devices on a single silicon wafer, by stacking a processed silicon device layer from a donor wafer on top of the active device layer of a starting silicon wafer. The unique advantage of the process

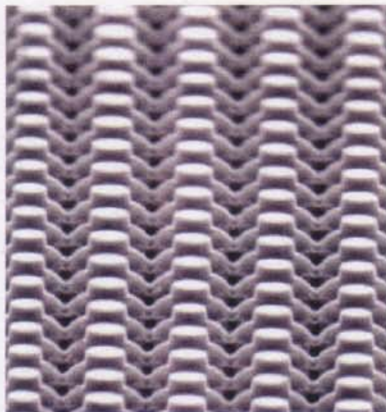

FIGURE 3. Portion of the 128M vertical transistor array, showing 0.8µm diameter pillars with surrounding gate conductor. *Courtesy of BeSang, Inc.*

is unrestricted 3D interconnection using conventional via technology, requiring neither wafer alignment nor TSVs.

For the demonstration units, the base wafer contains memory-control logic created with standard 180nm CMOS processes on 200mm wafers. Typical process temperatures are 850°C. The logic devices are finished with interconnection and via layers over the top surface.

The memory devices are created on a separate donor silicon wafer. It likewise is processed at 850°C to create the stacked doping layers required for vertical memory cells. The two wafers are bonded in a proprietary bonding process below 400°C, which transfers a single crystal doped silicon layer <1µm thick from the donor device to the base wafer. This transferred silicon layer is then patterned and metallized to create separate vertical transistor memory devices and connections.

The demonstration chips have 128M vertical transistors suitable for memory bit cells, positioned as a silicon layer with cells connected by simple vias to the control logic (Figure 3). In theory, the BeSang transfer process can be repeated to allow unlimited layer stacking. This creates high density stacking in the Z-axis, without resorting to increasingly painful shrinking in X and Y dimensions. The result could be significant cost and space savings.

Conclusion

Clearly, wide commercial availability of TSV is going to happen. When it does, TSV will have compelling advantages for interconnecting high performance, highly interconnected die, like microprocessors. However, most high-volume die stacking now is not in that category, nor is most expected to be there soon.

For example, Prismark Partner's 3D market forecast for 2011 is that 75% of 3D units will be in memory-only stacks, and about 80% of those will be 2-die and 3-die stacks. By 2011, the methods described here will be further down their cost curves, and perhaps unattractive targets for TSV replacement in these memory stacks. 3D stack-up is likely to long remain a multi-player, multi-technology game. **AP**

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